REMARKS

I. Introduction

In response to the Office Action dated November 29, 2005, Applicants have amended claims 1-3, 8, 12, 14 and 16-20. The limitations of claim 3 have been incorporated into claim 1. Claims 3 and 17-20 have been amended to indicate their status as independent claims including all limitations of the base claim and any intervening claims and to overcome the objections under 35 U.S.C. § 112, second paragraph. Claims 8, 12, 14 and 16 have been amended to show proper claim dependency on claim 3. Support for the amendment to claim 2 can be found, for example, on page 7, lines 9-12 of the specification. Support for amendments to claims 17 and 19 can be found, for example on page 12, lines 7-19 of the specification. No new matter has been added.

Applicants note with appreciation the indication of allowable subject matter recited by claims 3-7 and 17-20 by the Examiner. As claims 4-16 are dependent on independent claim 3, and claim 1 has incorporated the limitations of claim 3, Applicants assert that claims 1 and 3-20 are allowable over the cited prior art.

For the reasons set forth below, Applicants respectfully submit that all pending claims are patentable over the cited prior art references.

II. The Rejection Of Claim 2 Under 35 U.S.C. § 102

Claim 2 was rejected under 35 U.S.C. § 102(e) as being anticipated by Hidaka et al. (U.S. Patent 6,646,911). Applicants respectfully submit that Hidaka et al. fails to anticipate the pending claims for at least the following reasons.

With regard to the present invention, claim 2 recites, a semiconductor memory device comprising: a plurality of first memory cells arranged in matrix; a plurality of word lines each connecting a subset of the plurality of first memory cells which are aligned in a row direction; a

plurality of bit lines each connecting a subset of the plurality of first memory cells which are aligned in a column direction; and a plurality of second memory cells which are connected to at least either of the word lines and the bit lines, wherein the first memory cells and the second memory cells each have a charge storage portion for storing charges, and when a common voltage applied to the word lines or the bit lines of the first memory cells and the second memory cells, the amount of change in charges in the second memory cells is larger than the amount of change in charges in the first memory cells.

It is asserted that Hidaka teaches that when voltage application to the word lines or bit lines changes the amounts of charges stored in the charge storage portions of the first memory cells and the second memory cells, the amount of change in charges in the second memory cell is larger than the amount of change in charges in the first memory cell. As evidenced by Hidaka et al. (column 25, lines 27-67; column 26, lines 1-67; column 27, lines 1-24), the difference between the amount of change in charges in the first memory cell and the amount of change in charges in the second memory cell is caused by current difference applied to each memory cell by using switch circuit (Fig.19, 20).

In contrast, turning to amended claim 2, a common voltage is applied to the first memory cells and second memory cells. On the other hand, in Hidaka et al., the voltage applied to the first memory cells is different from the voltage applied to the second memory cells, and the switch circuit (330) determines which voltage is applied to the memory. Thus, Hidaka et al. at a minimum, fails to disclose the limitation recited in claim 2, that is, a common voltage applied to the word lines or the bit lines of the first memory cells and the second memory cells.

As anticipation under 35 U.S.C. § 102 requires that each element of the claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference,

Kalman v. Kimberly-Clark Corp., 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983), and at a minimum, Hidaka does not disclose that a common voltage is applied to the word lines or the bit lines of the first memory cells and the second memory cells, it is clear that Hidaka does not anticipate claim 2 of the present invention.

III. Conclusion

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication of which is respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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